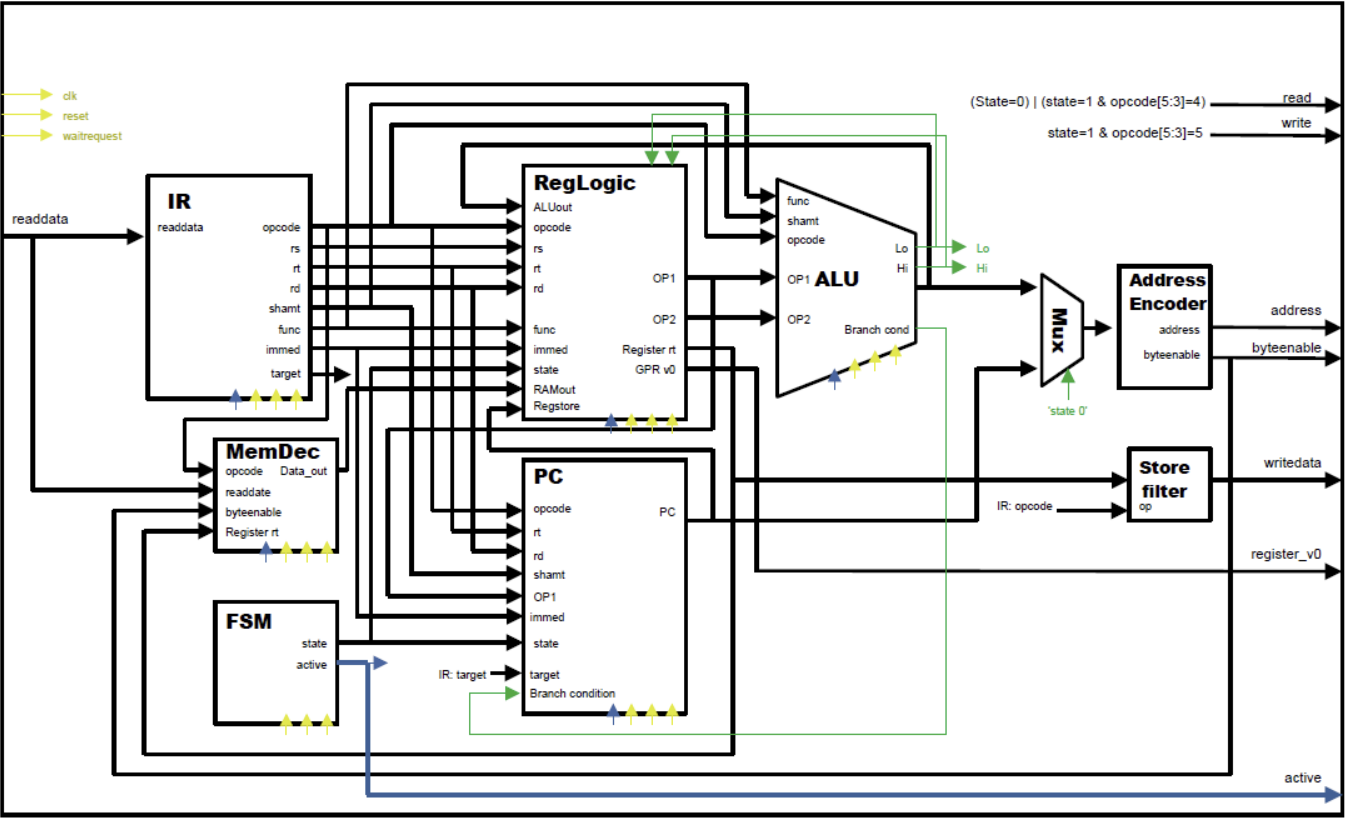
ELEC50010 Instruction Architecture & Compiler

The Second Quarter Coursework

Group6

**MIPS-compatible CPU Datasheet**

**Architecture**



**4**

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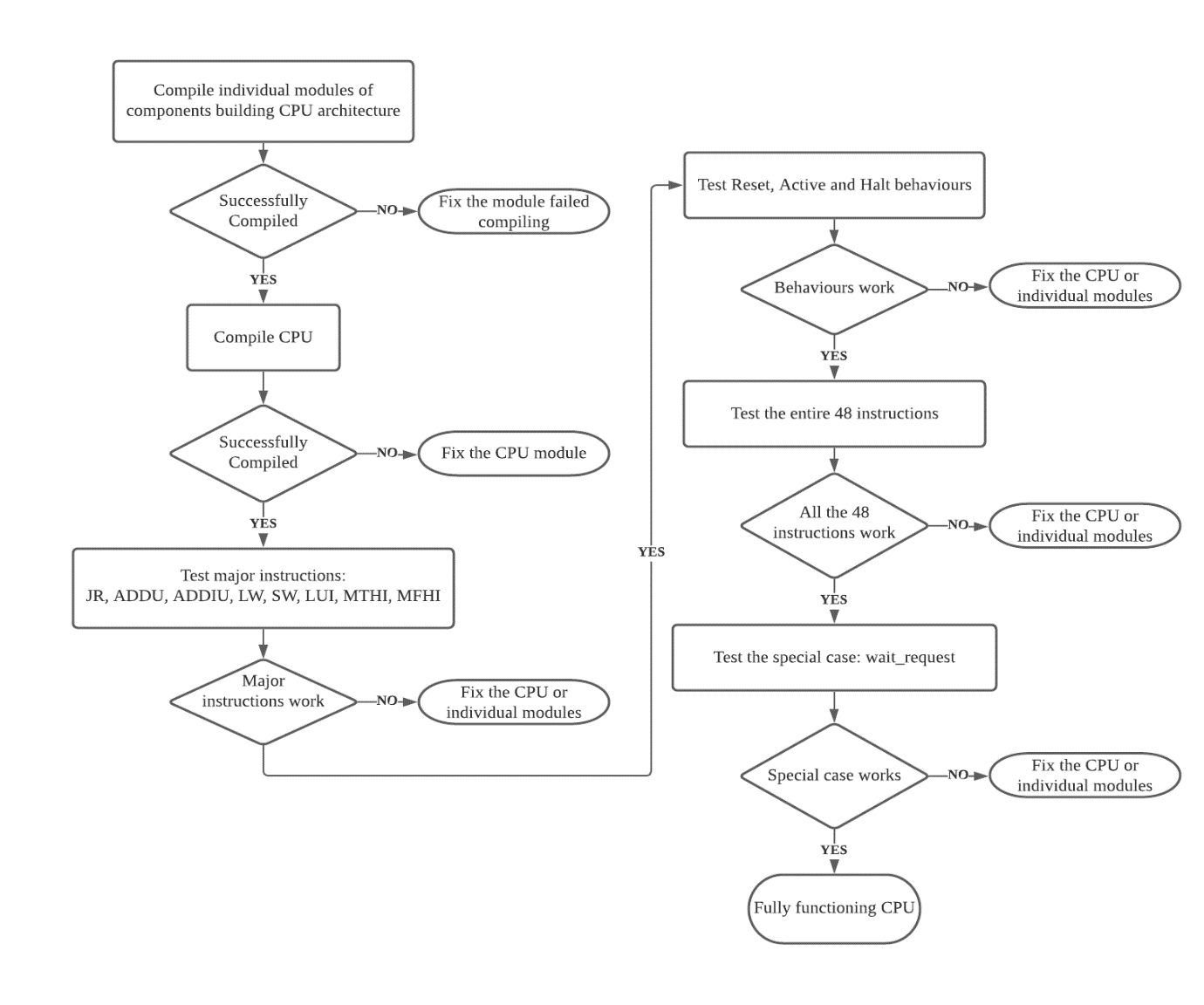
**Component analysis**

1. IR block
2. Finite State Machine
3. Memory Decoder
4. Register file and Control Logic Block
5. Program Counter
6. Arithmetic Logic Unit
7. Address Decoder
8. Store Filter

**Design Decision**

|  |  |
| --- | --- |
| Component Number | Design Decision & Purpose |
| ① | IR Block is designed to receive instruction input (32-bits) and provide opcode (6-bit), 1st register number (5-bits), 2nd register number (5-bits), destination register number (5-bits), shift amt (5-bits) and function code (6-bits) by performing sectional analysis. |
| ② | Finite State Machine is designed to receive memory address (32-bits) and opcode (6-bits) providing state (1-bit) and active (2-bits) as output.  The output state (2-bits) can represent 4 different states: Fetch, Decode, Execute and MEM/LINK. |
| ③ | Memory Decoder receives instruction input (32-bits), the value of 2nd register, rt (32-bits), opcode (6-bits) and byte-enable (4-bits) to produce RAM data out (32-bits) as an output depends on the byte-enable value.  Depends on the values of opcode (6-bits) and byte-enable (4-bits), the memory decoder performs I-type instruction. |
| ④ | Register file and Control Logic block receive ALU output (32-bits), opcode (6-bits), 1st register number, rs (5-bits), 2nd register number, rt (5-bits), destination register number, rd (5-bits), immediate (32-bits), shift amt (5-bits), function code (6-bits), RAM data out (32-bits) PC (32-bits) and state (2-bits). Depends on the opcode, it produces OP1 (32-bits), OP2 (32-bits), the value of the register rt (32-bits) and register v0 (32-bits). This component is an integrated component of register and control logic block. Once it receives an opcode, it checks whether the opcode is R-type or not and provides outputs by reading the register numbers and writing the address stored in the registers. |
| ⑤ | Program Counter is designed to receive opcode (6-bits), 1st register number, rs (5-bits), 2nd register number, rt (5-bits), destination register number, rd (5-bits), shift amt (5-bits), function code (6-bits), OP1 (32-bits), offset (16-bits), target (26-bits), control (4-bits), state (2-bits). Depends on the opcode (6-bits), the PC performs jump instructions such as jump (J) and branch instructions such as branch on equal (BEQ). |
| ⑥ | Arithmetic Logic Unit includes adder-subtracter logic block, multiplier block and divider block which performs addition, subtraction, multiplication, and division. Depends on the opcode (6bits), a suitable block will be chosen for the operation and provides ALU-out (32-bits), Lo (32-bits), Hi (32-bits) and branch-conditions (4-bits) as the outputs. |
| ⑦ | Address Decoder is designed to receive opcode (6-bits) and distinguishes the instructions into 4 types: load, store, link and other. Depends on the instruction type and opcode value, Address Decoder performs specific I-type instructions such as Load Byte (LB) and provides memory address (32-bits) and byte enable (4-bits) as the outputs. |
| ⑧ | Store filter is designed to receive opcode (6-bits) and performs I-type store instructions such as store byte (SB), store halfword (SH) and store word (SW) |

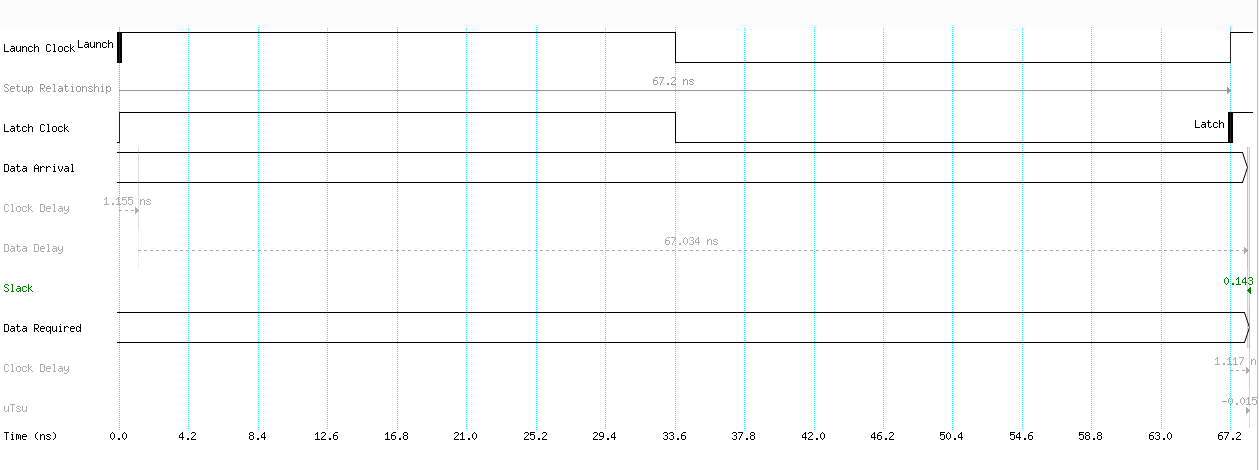
**Testing Approach – Flow Chart**



**Area and timing summary – “Cyclone IV E’ Auto” variant in Quartus**

Timing Summary

Waveforms



테이블이(가) 표시된 사진

자동 생성된 설명